REMARKS

Claims 15-17 and 19 remain for reconsideration. Claims 1-14 and 20-24 were previously cancelled. Claim 18 is herein cancelled.

This is a divisional application. A Preliminary Amendment was filed concurrently with the divisional application on March 24, 2004 canceling claims 1-14 and 20-24 and making a minor typographical correction to claim 15. The Preliminary Amendment appears in image file wrapper for this application in PAIR, but the Examiner appears to inadvertently missed it and examined all claims, including those cancelled. The claims above are as they appear after the Preliminary Amendment with additional amendment made to claims 15 and 19, and cancellation of claim 18. Thus, rejections made to the previously cancelled claims are herein omitted.

Thus, focusing on the pending claims, only two prior art rejections have been made as follows:

1. Claims 15-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. published application 2003/0076282 to Ikeda in view of applicants own admitted prior art (AAPA); and

2. Claim 19 stands rejected under § 103(a) as being unpatentable over Ikeda and the AAPA further in view of USP 5,907,314 to Negishi.

These rejections are respectfully traversed based on the following

discussion.

Briefly, embodiments are directed to increasing the functionality of an LOCOS imaging device. As shown for example in Applicant's so-called AAPA of Figures 1 and 2, a pixel array comprising pixels 14 and a liquid crystal material may be sealed between an Si substrate 11 and a glass plate 12 by an adhesive strip 16. Active circuitry, such as for, example, driver and memory circuits 18 may be located separately on the same chip. This arrangement wastes valuable chip real estate.

According to embodiments of the invention as, for example shown in Figure 4, Applicant's have invented a device which utilizes the area under the adhesive strip 41 that would otherwise be wasted. As shown in Figure 4, the frame buffer blocks FBB1 and FBB2 may be located at least partially under the adhesive strip 41 and may extend into the area within the adhesive strip; likewise for the external block 42 and the test block 44.

This architecture provides advantages as explained in paragraph [0028] wherein it states "*some embodiments of the invention include portions of the first and second frame buffers (FBB1 45 and FBB2 49), the associated first and second interface blocks (ICB1 46 and ICB2 48) and the control block (CB 43) located on the periphery of the die 40 and at least partially located within the area under an adhesive strip 41 that attaches the cover glass to the die 40, thus saving valuable die size. If the size and complexity of the device permits, it is preferable that the frame buffers are located completely within the area under the adhesive strip 41, thus providing increased functionality with no*

increase in die size" (emphasis added).

With regard to the primary reference to Ikeda, the Examine relies primarily on Figure 17A-B as showing Applicant's claimed invention. As discussed in Ikeda [0145]: *Then, the active matrix substrate on which the pixel portion, the driving circuit portion and the memory cell are formed is adhered to the opposing substrate using a sealant [sic. 3065]. Filler is mixed in the sealant [sic. 3065]. The filler and the spacers help the two substrates to be adhered to each other with a constant gap therebetween. After that, a liquid crystal material 3063 is injected between the substrates, and sealing agent (not shown) carries out full encapsulation. As the liquid crystal material 3063, a known liquid crystal material may be used. In this way, an active matrix liquid crystal display device as illustrated in FIG. 17B is completed.*

Thus, analogizing the "sealant" 3065* of Ikeda to Applicant's "adhesive strip 41" it is clear that no active circuitry, such as memory, is located "under the adhesive strip" or sealant 3065 of Ikeda.

Claim 15 has been amended to recite "..., the connection area defined by a generally rectangular adhesive strip; ... a frame buffer configured to store pixel data located at least partially under the

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* The text of Ikeda references the sealant as "3064"; however, this reference numeral does not appear to exist in the Figures including Figures 17A-B. It is presumed that the "sealant" is reference numeral 3065. This is logical since in Figure 18B, the sealant is 3206 which appears in generally the same position as 3065 in Figure 17B.

adhesive strip; a pixel array located completely within the connection area;... an external interface block data, located at least partially under the adhesive strip, ... and a control block data, located at least partially under the adhesive strip ..." (emphasis added).

The above highlighted features which save valuable chip real estate is not taught or suggested by either Ikeda, or the admitted prior art. Thus, a case prima facie obviousness is not been shown for claims as now presented. And the rejection should be withdrawn.

With regard to the rejection of claim 19, the Examiner has further relied on Negishi for showing a frame buffer, interface control block and pixel array divided into first and second parts. Without addressing the accuracy of that finding, it is noted that at a minimum, Negishi, like Ikeda and the AAPA, does not show, nor is it relied on to show or teach, active circuitry under the adhesive strip as now claimed. Thus, again, prima facie obviousness has not been shown.

The above features recited in the claims are not taught or suggested by the prior art of record. As such, it is respectfully requested that the outstanding rejections be withdrawn.

In view of the foregoing, it requested that the application be reconsidered, that claims 15-17 and 19 be allowed and that the application be passed to issue. Please charge any shortages and credit any overcharges to

Intel's Deposit Account number 50-0221.

Respectfully submitted,

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